A Practical Approach to Speech Processor for Auditory Prosthesis using DSP and FPGA

V.Bhujanga Rao
CC(R&D), DRDO HQ
Ministry of Defence,
Govt of Inida, Delhi
919866441074
vepcrew1@rediffmail.com

P.Seetha Ramaiah
Andhra University
Dept. of Computer Science and
Systems Engg,Vishakhapatnam, India
919848224505
psrama@gmail.com

K.Raja Kumar
Andhra University
Dept. of Computer Science and
Systems Engg, Visakhapatnam, India
919490132765
krajakumar@yahoo.com

ABSTRACT

Auditory prosthesis (AP) is a widely used electronic device for patients suffering with severe hearing loss by electrically stimulating the auditory nerve using an electrode array surgically placed inside the inner ear. The AP also known as cochlear implant (CI) mainly contains external Body worn Speech Processor (BWSP) and internal Implantable Receiver Stimulator (IRS). BWSP receives an external sound or speech and generates encoded speech data bits for transmission to IRS via Radio Frequency transcutaneous link for excitation of electrode array placed in the inner ear. Development of BWSP and IRS involves normally the use of either standard microprocessor or microcontroller or digital signal processor (DSP) or FPGA or ASIC devices. Sometimes the performance of the AP system using the standard processors cannot meet the requirement of the intended application. As the selected DSP processor (ADSP2185) from Analog Devices Inc. solely cannot perform the purpose of the speech processor for auditory prostheses, the Xilinx FPGA is added to fulfill the requirement. Combination of a standard processor such as DSP and FPGA may lead to the solution in both prototyping and target operational system. The ADSP2185 processor is used to realize the Continuous Interleaved Sampling (CIS) algorithm for speech signal processing and FPGA is used to realize the speech data encoding algorithm. This paper introduces practical implementations of digital speech processor for use in AP based on DSP ADSP-2185 and Xilinx's FPGA Spartan 3 with the description of practical data. The combination of ADSP2185 and FPGA is used to develop Speech Processor for an auditory prosthesis. FPGA implementation of speech data encoder is initially simulated using ModelSim and interfaced with ADSP2185. The entire embedded application is tested with real time speech signals by using laboratory model IRS and satisfactory results are observed.

Keywords: Auditory prosthesis/cochlear implant, Speech Processor, DSP, FPGA.

1. Introduction

Development of embedded applications normally requires the use of either standard microprocessor or microcontroller or digital signal processor (DSP). Design of embedded system involves the partition of target system into hardware and software implementation parts. The price and performance requirements represent major criteria to choose between hardware and software implementation of the solution. Standard single-chip microcomputers or DSP's often sufficient for application requirement, and only software has to be developed for a given application. If additional hardware interfacing is required, it is usually implemented using standard specialized chips, or using general MSI/SSI chips. This leads to a static solution and the PCB is to be redesigned for any alterations. Field-Programmable static RAM based Gate Arrays offer easy reprogrammability and change of the function without change of the PCB design using simple downloading of a new bit stream representing new circuit design. The feature of dynamic reconfigurability is used to change the dynamically the function of an FPGA in a time-multiplexed manner [1]. FPGA is a programmable logic device that supports implementation of relatively large logic circuits. DSPs are a type of specialized processor with customized architectures to achieve high performance in signal processing applications. DSPs usually include hardware support for fast arithmetic, including single cycle multiply instructions (often both fixed-point and floating-point),

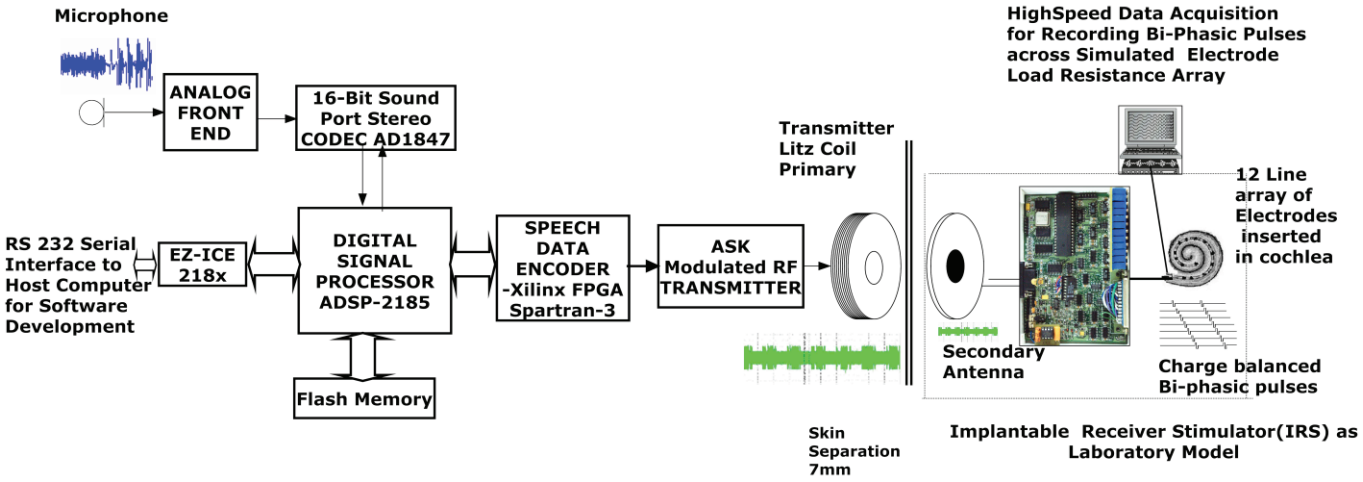

Figure 1: Functional block diagram of Speech Processor for Auditory Prosthesis.

large (extra wide) accumulators, and hardware support for highly pipelined, parallel computation and data movement. To keep a steady flow of operands available, DSP systems usually rely on specialized, high bandwidth memory subsystems. The complementary capabilities of DSPs and FPGAs integrated into high-density systems will continue to evolve to meet the growing challenges of high-complexity signal processing applications.

The auditory prosthesis has recently emerged as clinically acceptable prosthesis for aiding people who suffers from a profound to total sensorineural hearing loss. The multi-channel auditory prosthesis system, based on research undertaken at the Andhra University and Naval Science and Technological Laboratory, Visakhapatnam [2-5], uses an external BWSP and surgically implanted prosthesis to stimulate auditory neurons with biphasic pulses via an electrode array placed in the scala tympani of the cochlea (inner ear). The performance of the AP depends on the various parameters such as number of electrodes, placement of electrodes, types of electrodes, stimulation, and the speech processing strategies to deliver the important acoustic features to understand the sound under noisy environment. Development of high performance speech processor for auditory prostheses for AP involves careful selection of the parameters.

The development of auditory prostheses involves the potpourri of electronic systems, signal processing, mechanical engineering, physiology, electronics engineering and computer science and engineering [6-9]. Signal processing plays an important role in the development of different techniques for deriving electrical stimuli from the speech signal. Developing speech or sound signal processing algorithms that would help in mimicking the function of a normal cochlea in inner ear is the biggest challenge for the signal processing engineers. The function of Auditory Prostheses is an artificial replacement of damaged inner ear using external BWSP and IRS for stimulating auditory nerve via electrode array that enables understanding the speech by brain. The BWSP receives an external sound or speech and generates encoded speech data bits for transmission to receiver-stimulator via an inductive Radio Frequency (RF) transcutaneous link. The IRS receives the encoded speech data bits via RF receiver, decodes the speech data and electrically stimulates the corresponding electrode of line electrode array.

The working principle of the external BWSP is as follows: the microphone is used for picking up sound wave for converting into an electrical signal by a device – CODEC (CODER-DECODER). CODEC is basically a combination of a high speed ADC-DAC, which picks up analog sound signal from microphone, converts into digital samples and sent to the DSP for speech processing using CIS algorithm. The incoming sound signal is divided into 8 frequency bands (or channels) with center frequencies ranging from 250 to 7500 Hz. The output of each filter is rectified and low pass filtered with a cutoff frequency of 200 Hz. After computing all 8-filter outputs, maximum value of each output is logarithmically compressed to fit the patient's electrical dynamic range. The compressed information is sent to the Speech Data Encoder(SDE) where it receives the data bytes in parallel, encodes the stimulation parameters and sends data serially bit by bit to the RF transmitter. The RF transmitter is based on ASK modulation which modulates the incoming signal form SDE and transmitted to the prosthetic implant (IRS) through the RF inductive coils. The laboratory model for IRS consists of RF receiver, speech data decoder, current stimulator, switch matrix and simulated resistance electrode array. The RF receiver receives the ASK modulated serial speech data through RF Coils, demodulates and recovers the serial data. The recovered data signal is given to the speech data decoder in receiver-stimulator where data is decoded and the desired electrodes are stimulated in accordance with the stimulation parameters to activate the remaining auditory neurons in the inner ear, restoring hearing sensations partially.

Two DSP processors :Motorola DSP56001 operating at 32MHz and TMS32C50 operating at 40MHz are popularly used for implementing speech processing algorithms including communication protocol and speech data encoding without FPGA/CPLD[10-14]. This paper addresses the implementation of speech processor using ADSP2185 DSP processor and Xilinx Spartan 3 FPGA. FPGA implementation for communication protocol and speech data encoding is relatively easy with a flexibility to adapt for new receiver-stimulator that needs different data rates, protocol and encoding schemes. This may lead to improvement in performance.

Due to the processing limitations of the current selected DSP - ADSP2185, we add Xilinx based FPGA as a co-processor to perform the tasks that are not done by ADSP2185. The tasks that are less frequently changed are distributed to ADSP2185. The tasks that are frequently changed and the tasks that are to be modified regularly and for future additional functions are implemented in FPGA. The ADSP2185 performs the following functionalities on speech signal such as band pass filtering, rectification, low pass filtering and compression suitable for patient's dynamic range. The tasks of FPGA are to encode the compressed 8 BPF outputs and transmit the encoded information serially bit-by-bit via RF transmitter. In brief, the Speech processor performs the implementation of CIS algorithm and the FPGA performs the Speech Data Encoder functions. This paper offers a practical approach for embedded system design that builds upon the potential of Hardware-Software co-design methodology for FPGA based Speech Data Encoder. The hardware design issues for Speech Processor for Auditory Prosthesis (SPAP) are presented in section-2. Section 3 deals with the software design issues of SPAP. Finally, the experimental results are given in section 4.

2. Hardware Design Issues for Speech Processor.

The main functions of SPAP are speech signal processing, speech data encoding and transmission of encoded speech data to IRS via transcutaneous RF inductive link. The hardware design requirements of SPAP are : (i) to sample continuously speech or sound signals from environment by the microphone of analog front end that carries the speech or sound signal to the speech processor, (ii) Speech Processor processes the signal into n ($4 \leq n \leq 8$) different bands/channels corresponding to n active electrodes inserted in cochlea, based on CIS speech processing algorithm using CODEC and DSP, (iii) DSP generates 16 data bytes -(8 electrode number bytes with their respective 8 bytes of electrode current units that correspond to 8 spectral maximum values in 8 bands of sampled speech signal) continuously, (iv) 16 speech data bytes from DSP are transferred on interrupt basis to Speech Data Encoder(SDE) that encodes 16 speech data bytes as per the synchronous serial communication protocol format, (v) Encoded serial speech data bytes are used by ASK modulator for transmitting to the IRS via inductive RF communication link for

stimulating the electrodes inserted inside damaged cochlea. The hardware functional block diagram of BWSP is shown in Figure 1. The Analog Front End (AFE) is used to amplify the incoming low amplitude speech signal from microphone. SPAP receives the analog speech signal from AFE, extract the spectral and temporal information by implementing the most popularly used CIS Speech processing algorithm. The processed information is fed to the SDE where it is encoded for stimulation and transmitted serially to the ASK modulated RF transmitter. The RF transmitter is based on ASK modulation which modulates the incoming signal from speech data encoder and transmitted to the IRS of CI fabricated as laboratory model through inductively coupled coils.

2.1 Description of Hardware functional blocks

Analog Front End: Analog Front End consists of 2-stage pre-amplifier followed by Automatic Gain Control (AGC) and a last stage amplifier for amplifying the low amplitude incoming signal from microphone.

2.1.1 CODEC

Coder-Decoder chip AD1847 is used to sample and convert the incoming speech signal via AFE into a 16-bit digital value being processed by ADSP2185. The CODEC receives the amplified input signal from analog front end and samples the input sound signal with the sample rate of 11025 Hz specified in control register, and transmits serially to the ADSP2185 with the 16-bit mono format.

2.1.2 Speech Processor

ADSP-2185 receives the 16-bit sample of speech information from AD1847 CODEC via its serial port SPORT0, processes the sample based on 4 to 8 channel CIS speech processing algorithm (programmable 4 to 8 digital FIR band-pass filtering over incoming speech signal sample followed by full-wave rectification, FIR low-pass filtering and power law compression). The output of CIS algorithm is a sequence of 16 speech data bytes that corresponds to 8 channel/electrode number bytes with their respective 8 charge bytes and stored in data memory of ADSP-2185. Once 16 bytes are in data memory, ADSP-2185 interrupts SDE using the connection of active low IOMS output of ADSP2185 to active low input INT0 of SDE. SDE in its interrupt service routine receives 16 speech data bytes via programmable flags PF0 to PF7 of ADSP2185 connected to FPGA

2.1.3 SDE

The required tasks of SDE are to (i) receive the processed speech data bytes (EL# - Electrode Number, CH# - Electrode Charge) from ADSP2185 for sampled frame of speech signal, and store in the internal RAM, (ii) encode stored speech data bytes based on basic synchronous serial communication protocol format with single character sync byte and (iii) send serially each frame to the ASK modulated RF transmitter at high rate (>100Kbps) to meet the requirement of frame by frame reception of speech signal and frame by frame stimulation of electrodes without loss of data frame.

2.1.4 ASK Modulator

The output of SDE as serial data bits of processed speech signal is given as input to ASK modulator that generates ASK signal for wireless transmission to IRS. Wireless power and data from BWSP to IRS implant module are transcutaneously transmitted using inductively coupled RF link between the transmitter coil of BWSP and the receiver coil of IRS.

2.2 VHDL Model of Speech Data Encoder

VHDL model of the proposed SDE has been developed. Top level entity consists of 16 input ports as shown in Figure 2. Out of these eight inputs are served as data port pins for reading the processed speech data bits that contains the information about electrode number and its corresponding charge. As the selected DSP processor Analog Devices ADSP2185 solely cannot perform the purpose of the speech processor for auditory prostheses, the Xilinx FPGA is added to fulfill the requirement. Combination of a standard digital signal processor ADSP2185 and Xilinx FPGA Spartan–3 is used to implement Speech Processor. As a laboratory model ADSP2185 processor is used to realize the Continuous Interleaved Sampling (CIS) speech processing algorithm and FPGA is used to realize the speech data encoding. Interfacing between FPGA and ADSP2185 is shown in Figure 2. Eight data lines from ADSP2185 (D_0-D_7) is interfaced as 8 data lines to Spartan 3, four address lines (A_0-A_3) and two control lines (active low WR and active low IOMS). Data transfer from ADSP2185 to Spartan 3 is based on the interrupt (active low IOMS) initiated by ADSP2185 for every 1ms time interval with lowering the write signal after 8-bit data and 4-bit address is placed on the data and address lines.

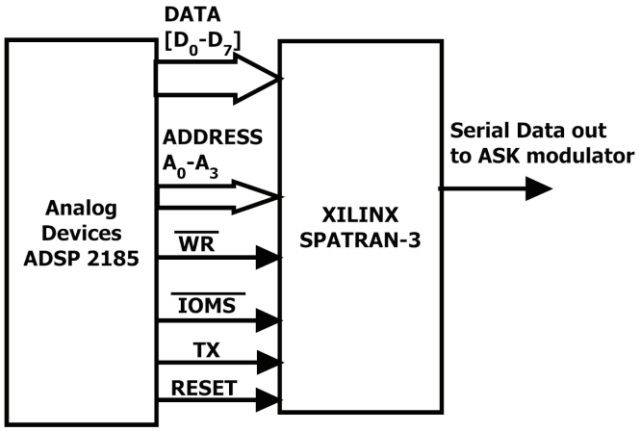

Figure 2: VHDL model of SDE interfaced with FPGA

3. Software Design Issues for Speech Processor

Software requirement for the operation of SPAP are given below

(i) CIS speech processing algorithm implementation
  (a) Digital FIR band pass filtering for speech data bytes received from CODEC by DSP
  (b) Envelope detection (Rectification and low pass filtering
  (c) Buffering 8 BPF outputs.

(ii) FPGA based SDE
  (a) Receiving and storing the processed speech data from ADSP2185
  (b) Speech data encoding as per synchronous serial communication protocol format

(iii) Serial data output for transmission of encoded speech data bytes for every 1mS speech sample.

These requirements are pictorially represented as a structured chart shown in Figure 3.

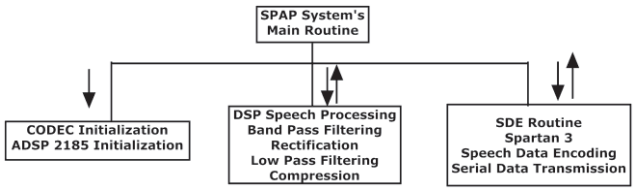

Figure 3: Structure chart for Speech Processor Software

3.1 CIS Speech processing algorithm implementation

The speech signal processing program for BWSP is developed as embedded program and coded in ADSP-2185 assembly language under EZ-KIT Lite/Visual DSP++3.5 IDE. CODEC is configured to sample the incoming speech signal at 11025 samples per second. There are 11025 samples /sec (i.e approximately 11samples for 1ms) as the speech input is sampled at 11.025 KHz. Since the selected electrode stimulation rate is fixed at 1000pps/channel, it is required to find sample value typically maximum in every 11 samples of every 1ms. Each received sample is processed in the following sequential stages: band-pass filtering, rectification, and low pass filtering. The temporal envelope in each channel is extracted with full-wave rectifier and low pass filters were designed to smoothen the amplitude variations with a cutoff frequency of 200Hz to allow maximal transmission of temporal envelope cues while avoiding aliasing when a relatively low carrier rates are used. After 11th sample is processed, ADSP2185 sends processed information of electrode numbers and charges of 8 channels to the SDE with 840 cycles of ADSP-2185 processor left as spare after CIS processing and communication with SDE leading to 1ms latency time from the input speech sample to an output bi-phasic pulse. A power-law transformation is used to map the relatively wide dynamic range of derived envelope signals onto the narrow dynamic range of electrically-evoked hearing. The acoustic envelope of amplitude '*x*' (1000 as minimum to exclude noise floor and 32565 as maximum of 15-bit value as per 1.15 format of ADSP2185 processor: 60dB to 90dB dynamic range) is mapped to the electrical amplitude '*y*' (1 to 255 of 8-bit unsigned value: 0dB to 48 dB) according to the power-law relation

$$y = Ax^p + B$$

The constants A and B are chosen such that the input acoustic range [x_{min} , x_{max}] is mapped to the electrical dynamic range [THL, MCL], where THL is the Threshold Hearing level and MCL is the Most Comfortable Level of hearing of the respective patient. Threshold is the highest stimulation at which no sound sensation occurs and ensure that the patient does not hear the THL level stimulation even in quite. Maximum Comfort Level is the highest stimulus level at which sound is loud but still comfortable. 50 for THL and 100 for MCL are chosen as default values for any patient. These stimulation levels ensure the safe and acceptable electrical stimulation levels to understand the speech/sound signals fitted by identification of THL and MCL with several iterations to adjust the speech processor for each individual patient by an experienced audiologist [16]. Actual values are programmed by the audiologist using clinical programming. For power law compression function, the constants A and B can be computed as follows:

$$A = \frac{MCL - THL}{x_{\max}^p - x_{\min}^p}$$

$$B = THL - Ax_{\min}^p \qquad \text{Where } p<=0.0001$$

After the power-law compression, every processed sample is compared with every previous processed sample and its maximum value is stored in the buffer until all samples are processed. The same process is carried out for all 8 channels that contain band-pass filtering, rectification, and low pass filtering with the same input sample.

The stored processed samples of all 8 channels are sent to the SDE via parallel interface. BWSP sends the processed information to SDE for every 1.00 milliseconds which in turn drive the electrodes (simulated electrode resistances) at 1000pps/electrode via transcutaneous RF link and IRS.

3.2 FPGA based implementation of SDE

The SDE has been implemented as speech data receiving and encoding on Xilinx Spartan 3. The register transfer level (RTL) description of the Speech Data encoder was implemented on Xilinx Spartan 3 using VHDL behavioral description. The SDE implementation consists of (a) Realization of a dual port RAM for storing the received processed speech data from ADSP2185 that contains the electrode number along with its corresponding excitation charge for 12 electrodes and (b) formats the processed speech data bits (Speech data encoding) as per synchronous serial communication protocol format and to implement parallel to serial converter to transmit the encoded data serially to the RF transmitter.

Table 1 - Device Utilization Summary (xc3s200-4pq208)

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	148	3,840	3%
Number of 4 input LUTs	286	3,840	7%
Logic Distribution			
Number of occupied Slices	225	1,920	11%
Number of Slices containing only related logic	225	225	100%
Number of Slices containing unrelated logic	0	225	0%
Total Number of 4 input LUTs	418	3,840	10%
Number used as logic	286		
Number used as a route-thru	132		
Number of bonded IOBs	12	141	8%
Number of BUFGMUXs	1	8	12%

The programs are realized to store the received data from the DSP unit into the Dual Port RAM, at the Xilinx- FPGA kit frequency and transmit the contents of RAM at 172kbps baudrate serially to the RF transmitter. Only after the data is read from all the 16 registers of the read port, it gets refreshed with the data present at that particular instant for the write port. All the data inputs are required for SDE are received from ADSP2185. The SDE performs two functions (a) store the data from D0-D7 of ADSP2185 and (b) transmits the data available on RAM serially to RF transmitter. The sequence of operations for storing the data is (i) IOMS signal should be low, which makes the enable of RAM high, as is passed through a NOT gate, (ii) Data available from D0-D7 are transferred to the register specified by the address line and (iii) write signal should be low during storing. After all the data bytes are stored in dual port RAM, the SP makes the transmit signal is high, the data stored on RAM is read and transmitted serially bit by bit. After all data stored in RAM are transmitted, the SDE is ready to receive the command from ADSP2185. A bit stream pattern was generated using VHDL model of the SDE and finally downloaded on Xilinx Spartan 3 FPGA chip using JTAG interface. Table-1 shows the resource utilization summary of Spartan 3 FPGA chip

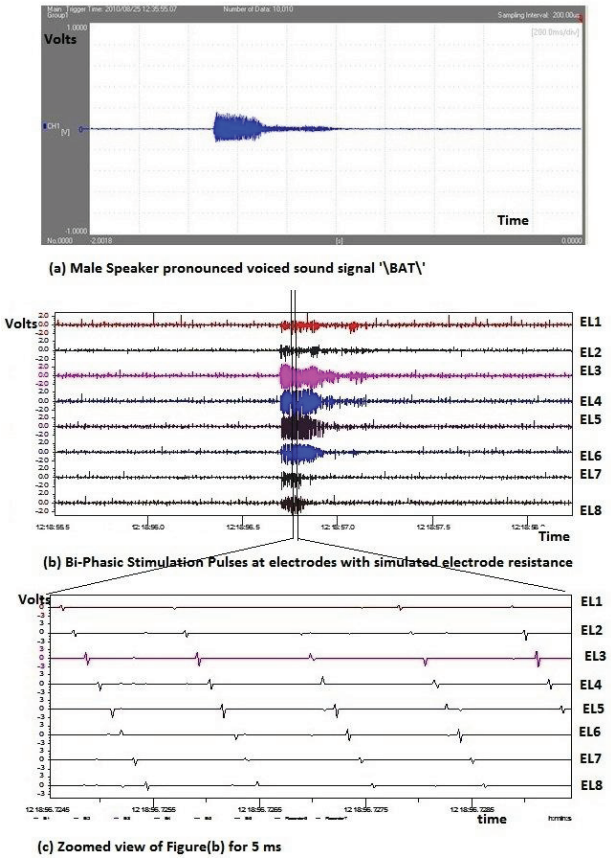

Figure 4. Measured waveforms at various points in the system. Top panel shows speech input token for vowel sound "BAT" measured at an output node of the analog preprocessor, and the middle panel show stimuli for the eight channels of stimulation with 5k resistors as loads. The bottom panel shows the interlacing of stimulus pulses using an expanded timescale. Waveforms in (c) are recorded as triangular instead of rectangular pulses due to the use of low speed data acquisition system (WaveBook 512A, IO Tech Inc, USA).

4. Experimental results

A Laboratory test station is arranged as a test setup to conduct testing experiments for a total CI system: BWSP, RF Link with variable inter-coil antenna distance from 5mm to 10mm, IRS, and load for electrode stimulation with i) 5KΩ resistive loads connected between eight active electrode nodes and reference electrode node in place of the twelve line electrode array and ii) an electrode line array of 12 platinum-iridium rings in ringer solution that exhibits impedance properties equivalent to electrode nerve interface. Several test experiments were conducted and the results recorded. The results were analyzed and found as expected. Figure 4 shows waveforms at various points in the CI system for the experiment of male speaker pronounced vowel sound "BAT". The top panel shows speech input ("BAT") measured in an output node of the analog front end and the middle panel shows stimuli of 8 channels with 5KΩ simulated electrode resistance loads. The bottom panel shows the most of the stimulation to 2, 3, 4, 5, and 6 electrodes and remaining electrodes 1, 7 and 8 electrodes with lower stimulation using an expanded time scale.

5. Discussions

The advantage of using FPGA's is that the embedded designer can create special purpose functional units that can perform limited intended tasks very effectively and efficiently. FPGAs can be reconfigured dynamically as well based on the requirement. FPGA based design is worth considering if the desired performance cannot be achieved using the DSP processor alone. The speech processor is designed as laboratory model for practical implementation of new speech processing algorithms in ADSP2185 DSP processor, protocols and encoding schemes in FPGA and their functional verification using SDE and RS. The BWSP is battery powered (3.7V, 3100mAH Li-Ion) with +5V generation using LM2621 (step-up DC-DC switching regulator) and overall current dissipation of the entire system is 150 mA that corresponds to 20 hours of continuous operation using 3100mAH lithium-ion rechargeable battery, allowing a patient to use the BWSP for a full day without recharging. The final product model of BWSP has dimensions as 110mm X 55mm X 30mm with the weight of 125grams, whereas Sprint speech processor of Cochlear Limited, Australia has dimensions of 103mm X 67mm X 23 mm with the weight of 146 grams [15] and Wearable Speech Processor of Nano Bioelectronics and Systems Research Center (NBS-ERC) of Seoul National University, Korea with dimensions of 82mm X 49mm X 19mm including the 1800 mAH rechargeable battery with approximately 17 hours of continuous operation[8].

6. Conclusion

The DSP and FPGA based speech processor for an auditory prosthesis is implemented. The speech processing algorithm CIS is implemented and processed information is encoded by FPGA based speech data encoder. FPGA based Dual-Port RAM for serial transmission is developed using VHDL. The parallel to serial transmission developed by using VHDL is verified by using high-speed data acquisition module WAVEBOOK and DasyLab software. FPGA based implementation is more attractive in the realization as the realization is more economical and easily reconfigurable. The cochlear implant product development (Indian Cochlear Implant System-ICIS) based on developed prototype model of CI System is ongoing by Defence R and D Organization - Naval Science and Technological Laboratory, Visakhapatnam with

the involvement of the following organizations: Teknosarus Embedded Systems Pvt. Ltd, Hyderabad for BWSP and Headset coil, Advanced Numerical Research and Analysis Group (ANURAG), Hyderabad for ASIC design and development and fabrication. Once the product is developed, plans are ongoing for animal testing and approval from Indian Health Authority – Central Drug Standards Control Organization (CDSCO). Implementation of the FPGA based complete SPAP is under progress with the aim of reducing the size and more features.

7. Acknowledgments

The findings reported in this paper form part of a joint project on development of cochlear implant device between Andhra University and Naval Science and Technological Laboratory, Visakhapatnam. The authors gratefully acknowledge the suggestions and insights provided by Prof Stephen J. Rebscher, University of California, San Fransisco, Prof B.S. Wilson, Adjunct Professor, PRATT School of Engineering, Duke University, Prof SJ Kim, School of Electrical Engineering and Computer Science and the Nano Bioelectronics Systems Research Center, Seoul National University and Prof. Philip Loizou, University of Texas, Dallas, during the development of prototype of CI System. The authors also acknowledge the invaluable and rich contribution of Mr. V.P. Rao, former Scientist-F and Mr. M. Mohan Krishna, Scientist-G of Naval Science and Technological Laboratory, Visakhapatnam during the development of CI System.

8. References

[1] F. Berthelot, F. Nouvel, and D. Houzet, "Design methodology for runtime reconfigurable FPGA: from high level specification down to implementation," in *Proceedings of IEEE Workshop on Signal Processing Systems (SiPS '05)*, vol. 2005, pp. 497–502, Athens, Greece, November 2005.

[2] K. Raja Kumar and P. Seetha Ramaiah, "Programmable Digital Speech Processor for Auditory Prostheses", Proceedings of IEEE International Region-10 Conference on Innovative Technologies for Societal Transformation – TENCON, 2008, November 18 - 21, 2008, Hyderabad, India.

[3] K. Raja Kumar and P. Seetha Ramaiah, "Microcontroller Based Receiver Stimulator for Auditory Prosthesis", Proceedings of IEEE International Region-10 Conference on Innovative Technologies for Social Transformation – TENCON, 2008, November 18 - 21, 2008, Hyderabad, INDIA

[4] K. Rajakumar and P. Seetha Ramaiah, "Personal Computer Based Clinical Programming Software for Auditory Prostheses", Journal of Computer Science, Vol 5. No. 8, pp. 589-595, 2009

[5] K. Raja Kumar and P. Seetha Ramaiah, "Development of Receiver Stimulator for Auditory Prosthesis", International Journal of Computer Science Issues, Vol. 7, Issue 3, No 2, May 2010.

[6] P. Loizou, "Mimicking the Human Ear: An overview of signal processing techniques used for cochlear implants," IEEE Signal Processing Magazine, 15(5), 101-130.

[7] Fan-Gang Zeng , "Trends in Cochlear Implants", Trends In Amplification Volume 8, Number 1, 2004, pp T1- T34.

[8] Soon Kwan An, Se-Ik Park, Sang Beom Jun, Choong Jae Lee, Kyung Min Byun, Jung Hyun Sung, Blake S. Wilson, "Design for a Simplified Cochlear Implant System", *IEEE Transactions on Biomedical Engineering*, vol. 54, no. 6,pp . 973-982, June 2007

[9] B. S. Wilson, S. Rebscher, F. G. Zeng, R. V. Shannon, G. E. Loeb,D. T. Lawson, and M. Zerbi, "Design for an inexpensive but effective cochlear implant," Otolaryngoly.—Head Neck Surg., vol. 118, no. 2, pp. 235–241, Feb. 1998.

[10] Zerbi, M. Wilson, B.S. Finley, C.C. and Lawson, D.T, "A Flexible Speech Processor Cochlear Implant Research", Proceedings of the Digital Signal Processing workshop, 13-16 Sep 1992, pp 5.7.1 - 5.7.2.

[11] Fontaine,R.;Alary,A.;Mouine,J.;Duval,F.; "A programmable speech processor for profoundly deaf people", Proceeding of the IEEE 17th Annual Conference Engineering in Medicine and Biology Society, 20-23 Sep 1995, Vol 2, pp 1617 – 1618.

[12] Bogli, H., Dillier, N. "Digital Speech Processor For The Nucleus 22-channel Cochlear Implant", Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 31 Oct-3 Nov 1991, pp 1901 – 1902.

[13] Hussnain Ali, *Member, IEEE,* Talha J. Ahmad, Asim Ajaz, and Shoab A. Khan, "Laboratory Prototype of Cochlear Implant: Design and Techniques", Proceedings of the 31st Annual International Conference of the IEEE EMBS, September 2-6, 2009, pp 803-806.

[14] Chen wei-bing ; Zhou ling-hong ; Wang lin-jing ; Xiao zhong-ju, "The Development of Six-Channel Speech Processor for Cochlear Implant Based on DSP", Proceedings of the 2nd International Conference on Bioinformatics and Biomedical Engineering, 2008. ICBBE 2008, 16-18 May 2008, pp 1613 – 1616.

[15] User Manual for the SPrint speech processor and accessories, Nucleus Cochlear Implant System, http://professionals.cochlearamericas.com/cochlear-products/nucleus-cochlear-implants/cochlear-implant-support-materials/user-manuals/user-man

[16] P.R.Deman, K. Daemers, M. Yperman, F. E., "Basic Fitting and Evaluation Parameters of a Newly Designed Cochlear Implant Electrode", Acta Otolaryngol 124, 2004, pp 281-285.