A Self Tuning Regulator based on the ARM Cortex-M4

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***Abstract*—The versatility and closed-loop performance resulting from the use of self-calibrating control systems are two of the most sought features when implementing a digital feedback loop based on embedded systems. However, such methods are typically based on computationally intensive algorithms that, when executed in low-cost embedded systems, severely restrict their usability to application with relatively slow dynamics in order to cope with the control-loop calculations turnaround time. Taking advantage of the new ARM Cortex-M4 microcontroller performance improvements in the digital signal processing field, this paper will present a real-time self-tuning regulator designed for a generic second order dynamic process. To assess the capabilities of this new architecture, a Buck DC-DC converter will be used as test scenario to present comparative measurements of the algorithm's turnaround time and CPU load under different system configurations and results relative to the setpoint tracking capability of the adaptive controller under time-varying dynamics.**

I. Introduction

In every dynamic system to be manipulated unexpected external disturbances and inherent uncertainties introduced by ageing effects, temperature variations or tolerances in the components can significantly change its operating conditions over the time. For that reason and in order to achieve the best performing results, self-calibrating capability is one of the most sought features when implementing a digital feedback control loop. Adaptive control theory [1] offers such robust solution, providing the groundings for the development of a self-compensating system withstanding a wider range of uncertainty when compared to standard control approaches. However, when a high frequency control loop is required, self-tuning techniques present challenging issues under the integration and feasibility point of view in embedded systems since their flexibility comes at the expense of increasing the computational resources necessary to deal with complex signal processing algorithms. For that reason, adaptive controllers are usually developed on complex and costly embedded systems such as Digital Signal Processors (DSP) [2] or Field-Programmable Gate Array (FPGA) [3] that require deep knowledge on low level / hardware specific programming languages to efficiently implement such algorithms.

To tackle the high performance algorithmic needs in low-cost embedded designs and soften the learning curve often required during the development stage, ARM recently introduced in the market a new processor family - the ARM Cortex-M4. This new microcontroller (MCU) family stands in the state-of-the-art of embedded systems by adding a set of instructions optimized for digital signal processing operations, a single cycle Multiply and Accumulate (MAC) unit and a single precision hardware Floating-Point Unit (FPU) to the broadly used general purpose, low-cost and low-power ARM Cortex-M3 and M0 families.

To demonstrate the performance improvements brought by this new microcontroller family, the present work will implement a generic adaptive controller for a second order system. Section II will briefly introduce the implementation of a real-time self-tuning regulator, and section III an application scenario based on a Buck DC-DC converter is used to evaluate the implemented regulator. The most relevant findings and final remarks of the presented work will be summarized on section IV.

II. Development of an adaptive controller

According to Åström and Wittenmark, to adapt means *to adjust a behaviour to conform to new environment* [1]. Self Tuning Regulators (STR) are one particular type of adaptive controllers developed according to such premise, being its generic block diagram depicted in the figure 1.

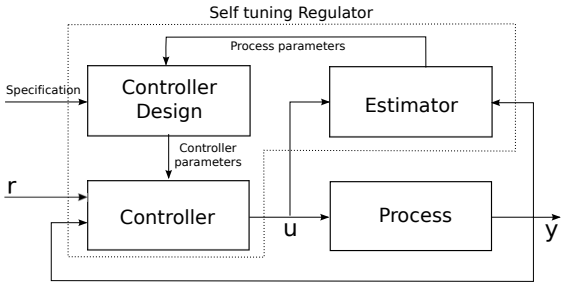

Figure 1. Block diagram of a Self Tuning Regulator

A self-tuning regulator can be seen as two feedback loops control problem: the typical feedback loop composed by a process to be manipulated and the controller responsible for the accomplishment of the manipulation goals; and an outer loop comprising a on-line model estimator and a controller synthesis block that dynamically adjusts the controller gains at each sampling period. The considerations taken into account during the development of the model estimator and controller synthesis will be discussed in the following two subsections.

A. Recursive identification of linear models

When a model to be identified is linear on its parameters, model extraction methods based on the squared error minimization such as the Recursive Least Squares (RLS) algorithm

are known to provide the best convergence proprieties to the solution that closely approximates a system input/output behaviour [7]. However, it is known that the conventional formalization of the RLS lacks the required adaptability to track time varying parameters so modified versions of the cited algorithm introduced an exponential weight that reduces past samples significance according to their obsolescence [7]. In practical scenarios where the system excitation is insufficient or not uniform over the whole parameters' space, this information loss mechanism ultimately leads numerical stability problems due to a phenomenon referred in the literature as covariance matrix windup [7]. Several heuristics have been proposed to adjust the information loss mechanism over the time but, for its simplicity, robustness and capability of maintaining the estimator adaptability to fast and slow parameter's variations, the Directional Forgetting mechanism [8], [9] stands as a superior and preferred approach. For that reason, the Recursive Least Squares with Directional Forgetting (RLSDF) estimator will be used in the present work and is briefly presented as follows.

Considering a discrete time-system with output $y(k) \in \mathbb{R}^1$ and the associated linear predictor $\hat{y}(k) = \varphi(k)\hat{\theta}(k)$, where the $\varphi(k)$ is the n-dimensional observation vector and $\hat{\theta}(k)$ is the n-dimensional model parameter's vector, the parameters' vector estimation can be recursively performed using the RLSDF algorithm as follows in equation 1.

$$\hat{\theta}(k) = \hat{\theta}(k-1) + K(k)\varepsilon(k) \ . \tag{1a}$$

$$\varepsilon(k) = y(k) - \varphi(k)^T\hat{\theta}(k) \ . \tag{1b}$$

$$r(k) = \varphi^T(k)P(k-1)\varphi(k) \ . \tag{1c}$$

$$K(k) = \frac{P(k-1)\varphi(k)}{1 + r(k)\alpha(k)} \ . \tag{1d}$$

$$P(k) = P(k-1) - K(k)\varphi^T(k)\alpha(k)P(k-1) \ . \tag{1e}$$

$$\alpha(k) = \begin{cases} \lambda_{df} - \dfrac{1-\lambda_{df}}{r(k)}, & r(k) > 0 \ . \\ 1, & r(k) = 0 \ . \end{cases} \tag{1f}$$

The parameter λ_{df} represents the algorithm forgetting factor and it is usually chosen in the interval $0.95 \leq \lambda_{df} \leq 1$. The choice of this parameter establishes a commitment regarding the algorithm's capability in tracking fast/slow variations of the model parameters.

Assuming that the process to be identified is described by the single-input, single-output (SISO) system presented in equation 2, the coefficients of the polynomials functions in the forward shift operator q, $A(q)$ and $B(q)$, can be obtained by the referred system identification method.

$$A(q)y(k) = B(q)u(t) \ . \tag{2}$$

B. Implementing a controller following a pole-placement approach

Based on the discrete model parameters given by the model estimator, the pole-placement technique will allow the synthesis of a control function by specifying the location of the closed-loop poles according the desired system closed-loop dynamics. Such control function will follow the structure presented in equation 3,

$$R(q)u(k) = T(q)r(k) - S(q)y(k) \ . \tag{3}$$

where R(q), S(q) and T(q) are polynomial functions, and u(k), r(k) and y(k) are the control, setpoint and output signals respectively. Replacing the equation 3 in the discrete time model of the system given by 2 and imposing some constraints to the unknown controller's polynomials, the control law synthesis problem resumes itself to find the solution of the equation 4 (where the polynomials B_m and A_m represent the desired closed-loop transfer function).

$$\frac{BT}{AR + BS} = \frac{B_m}{A_m} \ . \tag{4}$$

Verifying the causality criterion among relevant polynomials, assuring the controller's integral action to achieve null error in steady state, choosing the appropriate controller bandwidth for disturbance rejection and avoiding the cancellation of unstable open-loop zeros will provide the necessary restrictions to the controller synthesis problem. Assuming the controlled model as a pure second order system, the solution for this problem can be found algebraically. While being less flexible due to its *a-priori* assumptions, this approach is more computationally efficient and, for that reason, it was used in the evaluative scenario further depicted in this work. The obtained controller parameters are not here presented but can be found thoroughly presented in [1].

III. USE-CASE SCENARIO

To assess the performance improvements introduced with the Cortex-M4 based microcontrollers and the flexibility of the adaptive controller in time-varying conditions, an experimental setup was assembled based on a NXP LPC4337 microcontroller development board and a Buck DC-DC converter. The developed control software was implemented under a multitasking architecture managed by the FreeRTOS kernel[11].

The Buck converter, depicted in the figure 2, is one particular type SMPS that efficiently implements a regulated voltage step-down stage from an unregulated and possibly floating voltage source.

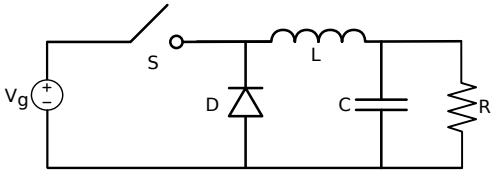

Figure 2. Diagram of the buck converter power stage

Due to its switched operation and possible fluctuations on the input voltage or load resistance, this system is considered

as non-linear and time variant. However, as proposed by the works of Vorperian [4] and Erikson[5], by using a switching frequency much higher than the power stage natural frequencies, one may assume that the changes in its natural response over a single switching period are relatively small at a specific operation point and use a locally linear second order model to describe the system's control-to-output voltage behaviour, as shown in equation 5.

$$H_D(s) = \frac{V_{out}(s)}{D(s)} = \frac{V_g/LC}{s^2 + s/RC + 1/LC} \; . \qquad (5)$$

The buck converter used during this evaluation was composed by a $680uH$ inductor, a $470uF$ capacitor and a 12V nominal input voltage. The switching frequency was $20KHz$, and the converter's load was chosen so it is always operating in the Continuous Conduction Mode. The following subsections will describe two evaluative scenarios highlighting the Self Tuning Regulator and the microcontroller's performance.

A. Voltage control of Buck converter

To evaluate adaptive controller performance under time varying conditions, a buck converter was tested under different operating points by changing its setpoint (between 3V and 8V) and randomly varying its resistive load (5.6Ω or 13Ω). The controller parameters were chosen so the system's closed-loop response presents a fast and nicely damped response, as obtained with a second order transfer function with natural frequency $\omega_0 = 600\,rad/s$ and damping coefficient $\zeta = 1$. Identically, the observer dynamics (which influence the system's response to eventual disturbances) were defined by a second order transfer function with natural frequency $\omega_0 = 1200\,rad/s$ and damping coefficient $\zeta = 1$. The presented results were logged by the microcontroller and transferred in real time to a Matlab ethernet socket at 1KHz sampling rate.

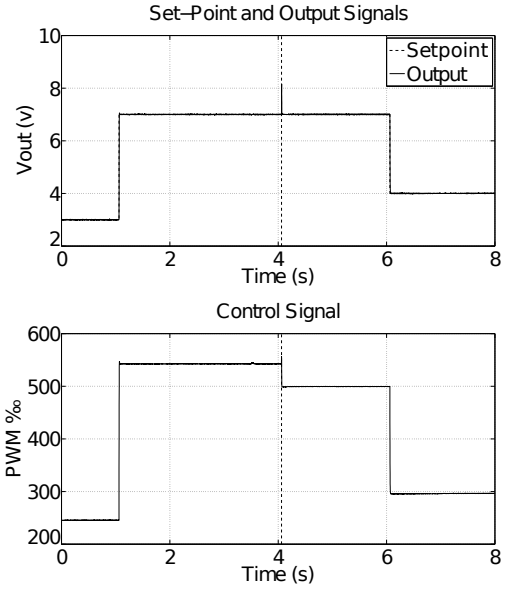

Figure 3. Output voltage response and control signal over 3 setpoint (3V, 7V and 4V), with a load variation from 5.6Ω to 13Ω (vertical dashed line) after 4s

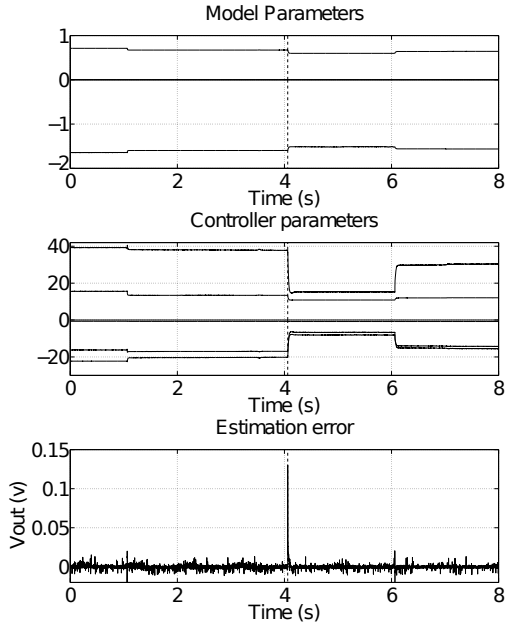

Figure 4. Estimator/controller parameters and estimation error over 3 setpoint (3V, 7V and 4V), with a load change from 5.6Ω to 13Ω (vertical dashed line) after 4s

As it can be found from figures 3 and 4, to each setpoint and load change corresponds a slight variation of the model parameters, assessing its variability with the operating conditions. Accordingly, the controller parameters are adapted in order to maintain the desired system's closed-loop performance.

The excellent reference tracking capability of this system is better depicted in the following two figures. In figure 5, the details of the system response to a setpoint variation from 3V to 7V are on focus, being measured a rise-time of approximately 5.3ms which closely matches the expected theoretical value of 5.6ms sought by the imposed closed-loop dynamics. Finally, the figure 6 depicts the system response to the load variation, showing the ability of the controller to stabilize the output voltage under 10ms.

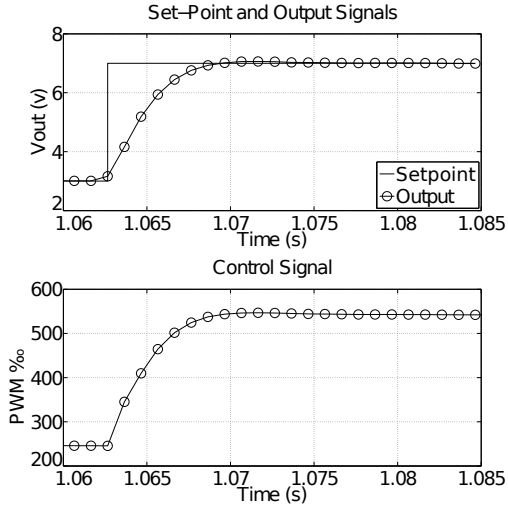

Figure 5. Detailed view of the system response to a setpoint variation from 3V to 7V.

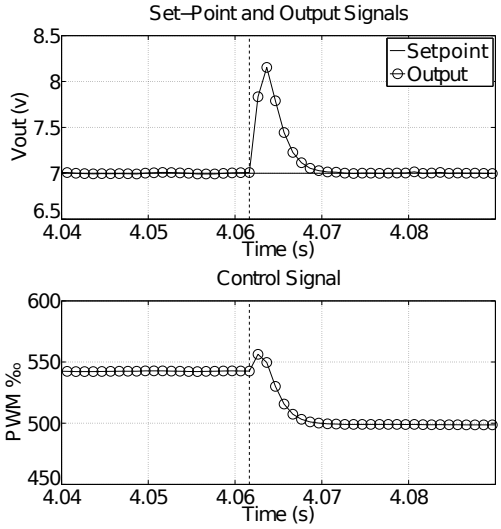

Figure 6. Detailed view of the system response to a load variation from 5.6Ω to 13Ω (vertical dashed line)

B. Algorithm turnaround time and CPU load

Putting into perspective the system's performance when solving computationally intensive mathematical algorithms, Table I presents the measured turnaround times for the RLSDF and the whole adaptive control algorithm under different scenarios and the CPU load measurements when executing the control system tasks at 5KHz rate. The Cortex-M4 core is configured to run at its maximum operating frequency (204 MHz) and the measurements were taken considering the execution of the required floating-point computations either by using the standard C floating-point emulation library or using the available hardware FPU. To establish a better comparison with a previous generation microcontroller, the same code was executed in a Cortex-M3 NXP LPC1759 operating at its maximum core speed of 120MHz.

	CM4 with Hardware FP	CM4 with Software FP	CM3 with Software FP
RLSDF	$5.86\mu s$	$43.20\mu s$	$74.12\mu s$
RLSDF + Pole Placement	$6.91\mu s$	$59.01\mu s$	$101.41\mu s$
Control Task CPU load	4.2%	35.3%	NA
Total CPU load	13.1%	63.2%	NA

Table I. ALGORITHMS' TURNAROUND TIME AND CPU LOAD MEASUREMENTS

As it can be found from the presented results, the RLSDF identification algorithm consumes a great fraction of the adaptive controller algorithm turnaround time due to the high number of mathematical operations required. Additionally, and meeting our initial expectations, the Cortex-M4 hardware FPU significantly enhanced the microcontroller's performance, reducing the algorithms turnaround time by a factor of approximately 8 when comparing to its execution using the available software floating point emulation libraries. This improvement is more significant when comparing with the Cortex-M3 core, where a factor of approximately 14 was verified. As a direct consequence, in the evaluated use-case the CPU load was significantly lowered, leaving sufficient headroom to apply the present control algorithm to systems requiring higher control rates. CPU load measurements relative to the Cortex-M3 core were not presented since the control tasks were not schedulable under the requirements of the system under evaluation.

IV. CONCLUSION

In this paper, the development of a versatile and robust self-calibrating control system in a microcontroller was assessed. The performance improvements achieved with the hardware FPU significantly contributed to the reduction of the algorithms turnaround time, leaving sufficient headroom for the system to cope with the overhead introduced by important additional system features such as a real-time kernel.

Regarding the adaptive controller versatility, by solely specifying the expected system model order and its desired closed-loop dynamics, the developed self tuning regulator shown its superior setpoint tracking and robustness performance against load disturbance and parameters uncertainty. This controller synthesis approach clearly demonstrated its advantages over traditional tuning methods found in the literature.

One can say that such powerful microcontrollers will potentially expand the possible usage scenarios of advanced algorithms in embedded applications, leading to the development of quicker and better control loops capable of coping with physical systems with faster dynamics.

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REFERENCES

[1] Åström, K., Wittenmark B.: Adaptive Control. Dover (2008)

[2] Sadinezhad, I., Angelidis, V.: On Optimizing DSP Implementation of the Recursive-Least-Squares Technique for Real-Time Power System Applications. In: IECON - 37th Annual Conference on IEEE Industrial Electronics Society, pp. 640 - 645, (2011)

[3] Morroni, J., Corradini, L., Zane, R., Maksimovic, D.: Adaptive Tuning of Switched Mode Power Supplies Operating in Discontinuous and Continuous Conduction Modes. In: IEEE Transactions on Power Electronics, vol. 24, issue 11, November (2009)

[4] Vorperian, V.: Simplified Analysis of PWM Converters Using Model of PWM Switch, Part I. Continuous Conduction Mode. In: IEEE Transactions on Aerospace and Electronic Systems, vol.26, issue. 3, (1990)

[5] Erikson, R., Maksimovic, D.: Fundamentals of Power Electronics, Second Edition. Kluwer (2002)

[6] Åström, K., Wittenmark B.: Computer Controlled Systems - Theory and Design. Prentice Hall, (1990)

[7] Ljung. L.: System Identification: Theory for the User. Pearson Education (1998)

[8] Hägglund, T.: New Estimation Techniques for Adaptive Control, PhD Thesis, Department of Automatic Control, Lund Institute of Technology, (1983)

[9] Kulhavý, R.: Restricted Exponential Forgetting in real-time identification. IFAC Symp. on Identification and System Parameter Estimation, pp. 1143-1148, (1985)

[10] Bin, Z., Guang-Ren, D., Zhi-Bin, Y.: Unified Parametrization for the Solutions to the Polynomial Diophantine Matrix Equation and the Generalized Sylvester Matrix Equation. In: Chinese Control and Decision Conference, (2008)

[11] FreeRTOS (website): www.freertos.org. Accessed on 24 January 2014